IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 08/886,388
Filing Date ..... July 1, 1997
Inventor ..... Gurtej Sandhu et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2811
Examiner ..... S. Crane
Attorney's Docket No. MI22-713
Title: Capacitor Constructions (As Amended)

#28
Appeal Brief
TRIED JONES
8-7-01

APPEAL BRIEF

To: Assistant Commissioner for Patents
Washington, D.C. 20231

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Appellants appeal from the final rejection, dated February 27, 2001, of claims 44, 45, 51-54, 56, 58-60, 62, and 66-68. This brief is submitted in triplicate in support thereof. A check in the amount of $310.00 in payment of the fee required under 37 C.F.R. §1.17(c) for filing a brief in support of an appeal is attached.

REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to appellants, the appellants' legal representative, or any assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF THE CLAIMS

Claims 44, 45, 51-54, 56, 58-60, 62 and 66-68 are pending. Claims 1-43, 46-50, 55, 57, 61 and 63-65 have been canceled. Claims 44, 45, 51-54, 56, 58-60, 62 and 66-68 stand finally rejected. The claims being appealed are claims 44, 45, 51-54, 56, 58-60, 62 and 66-68.

STATUS OF AMENDMENTS

The status of amendments filed subsequent to the final rejection is as follows: no amendments to claims 44, 45, 51-54, 56, 58-60, 62 and 66-68 were made after the final rejection dated February 27, 2001.

SUMMARY OF INVENTION

This application is a divisional application of U.S. Patent Application Serial No. 08/582,385, now U.S. Patent No. 6,218,237.

One aspect of the invention provides a pair of adjacent stacked capacitors fabricated using a photolithographic process having a characteristic minimum photolithographic feature dimension on a semiconductor substrate. The adjacent stacked capacitors each respectively

include a lower plate. The lower plates have a minimum lateral spacing from one another which is less than the minimum photolithographic feature dimension. Each lower plate comprises a polysilicon plug having a diameter that is less than the minimum photolithographic feature dimension. Each lower plate also includes at least two laterally opposed fins interconnected with and projecting laterally from the plug.

ISSUES

1. Whether claims 44, 45, 51-54, 56, 58-60, 62 and 66-68 contain subject matter not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention.

2. Whether claims 44, 45, 51-54, 56, 58-60, 62 and 66-68 are indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

3. Whether claim 44 is unpatentable over Morihara et al., "Disk-Shaped Stacked Capacitor Cell For 256 Mb Dynamic Random Access Memory" (Jap. J. App. Phys., Vol. 33, (1994), Pt. 1, no. 8, pp. 14-19, in view of S. Wolf and R. Tauber, "Silicon Processing For the VLSI Era, Vol. 1: Process Technology", p. 493 (Lattice Press, Sunset Beach, CA, copyright 1986).

4. Whether claims 44, 45, 51-54, 56, 58-60, 62 and 66-68 are unpatentable over Morihara et al., "Disk-Shaped Stacked Capacitor Cell For

256 Mb Dynamic Random Access Memory" (Jap. J. App. Phys., Vol. 33, (1994), Pt. 1, no. 8, pp. 14-19, in view of S. Wolf and R. Tauber, "Silicon Processing For the VLSI Era, Vol. 1: Process Technology", p. 493 (Lattice Press, Sunset Beach, CA, copyright 1986) and further in view of Lee, U.S. Patent No. 5,684,316.

GROUPING OF CLAIMS

Claims 44, 45, 51-54, 56, 58-60, 62 and 66-68 stand or fall alone as one group.

THE REFERENCES

1. Morihara et al., "Disk-Shaped Stacked Capacitor Cell for 256 Mb Dynamic Random-Access Memory", Jpn. J. Appl. Phys. Vol. 33 (1994), Pt. 1, No. 8, pp. 14-19.

Morihara et al. describe a memory cell structure using disk-shaped capacitors to form a 256 Mb DRAM. The capacitor structure is formed on a sidewall of a cylindrical storage node by a self-aligned process. A distance between adjacent storage node patterns (disc edges) of 0.1 micron can be achieved which is smaller than a minimum photolithographic feature size.

2. S. Wolf and R. Tauber, "Silicon Processing For The VLSI Era, Vol. I: Process Technology", p. 493 (Lattice Press, Sunset Beach, CA, copyright 1986).

This page is cited by the Examiner to compare minimum lithographic feature sizes for different lithographic technologies at the time of printing of the reference.

3. J-Y. Lee, U.S. Patent No. 5,684,316.

Lee describes a semiconductor memory device including capacitors formed above and below a cell transistor. The cell includes first and second transistors formed in a first level and a first storage electrode connected to the first transistor and formed below the first level. A second storage electrode is connected to the second transistor and is formed above the first level. The capacitor electrodes are connected to the transistors by spacers formed on sidewalls of each transistor source. Undercuts are formed between the storage electrode and the transistor.

ARGUMENT

Issue 1. The Examiner's position, insofar as understood, is that the claims are not enabling for processes that may be developed after the filing date of the application. However, Applicants are not required to provide an application that is enabling for dates after the filing date of the application, for the simple reason that to attempt to do so is absurd.

Additionally, the Examiner has repeatedly mischaracterized Applicant's claims as being product-by-process claims because the claims include language intended to provide context for the concept of "minimum feature size". To clarify the subject matter of the claims, Applicants are not claiming any photolithographic process and do not recite process steps in the claims.

Specification Must Be Enabling As Of The Filing Date

Applicants note the requirements of MPEP §2164.05 (a), entitled "Specification Must Be Enabling As Of The Filing Date". This MPEP section specifically states that "The state of the art at the filing date of the application is used to determine whether a particular disclosure is enabling as of the filing date. Publications dated after the filing date providing information publicly first disclosed after the filing date generally cannot be used to show what was known at the time of filing."

The Examiner cites Wolf to show the state of the art in 1986 and compares this to the state of the art shown by Morihara et al. in 1994. The Examiner then hypothesizes that further improvements in the state of the art will occur. In effect, the Examiner is improperly using a hypothetical publication to show further progress in the lithographic arts after the filing date of the application to reject the claims. Such is clearly highly improper.

This MPEP section also states that "The state of the prior art provides evidence of the degree of predictability in the art and is related to the amount of direction or guidance needed in the specification as filed to meet the enablement requirement." Applicants have previously pointed out that some aspects of the lithography arts are extremely predictable to those of skill in the art.

Specifically, a minimum photolithographic feature size does characterize all lithography processes now known and will characterize all lithography processes that will be developed. Applicants have extensively demonstrated, using tools available to the Examiner, that this terminology is

regularly and routinely used in the relevant arts and is understood by those of skill in the art.

Enablement Commensurate In Scope With The Claims

Applicants further note the requirements of MPEP §2164.08, entitled "Enablement Commensurate In Scope With The Claims". This MPEP section quotes *In re Goffe*, 542 F.2d 564, 567, 191 USPQ 429, 431 (CCPA 1976), where the court states that "[T]o provide effective incentives, claims must adequately protect inventors. To demand that the first to disclose shall limit his claims to what he has found will work or to materials which meet the guidelines specified for "preferred" materials in a process such as the one herein involved would not serve the constitutional purposes of promoting progress in the useful arts."

Accordingly, the Examiner's position fails to conform to the law, which the Examiner is, contrary to her stated position, obligated to follow via the principle of stare decisis. Moreover, by taking a position that is contrary to law, the Examiner is improperly depriving Applicants of a constitutionally-granted property right.

Inconsistent Application of Arbitrary Standards

Moreover, applying the standard of enablement that the Examiner currently is using, for example, against previously issued patents, it is abundantly clear that many of the past U.S. patents would be unpatentable under 35 U.S.C. 112 for exactly the same reasons that the instant application has been improperly rejected.

In fact, the very same Examiner's name appears on U.S. Patent No. 6,150,687, issued to Noble et al., entitled "Memory Cell Having A Vertical Transistor With Buried Source/Drain And Dual Gates", filed on July 8, 1997; U.S. Patent No. 6,037,620, issued to Hoenigschmid et al., entitled "DRAM Cell With Transfer Device Extending Along Perimeter Of Trench Storage Capacitor", filed on June 8, 1998; and U.S. Patent No. 6,025,624, issued to Figura, entitled "Shared Length Cell For Improved Capacitance", filed on June 19, 1998. Each of these patents resulted from an application that was filed after the instant application. Further, each of these patents state on their face that they were examined under the aegis of Examiner S. Crane. Each of these patents includes recitation of a "minimum feature size" or language equivalent thereto in defining the subject matter claimed.

Specifically, claim 10 of U.S. Patent No. 6,150,687 recites that "the integrated circuit surface are of the memory cell is $4F^2$, where F is a minimum feature size".

Claim 2 of U.S. Patent No. 6,025,624 states that "the area occupied by said cell on a substrate is less than or equal to about 4.5 F^2, wherein F is defined as minimum lithographic feature size", claim 3 states that "the area occupied by said cell on a substrate is less than or equal to about 4.0 F^2, wherein F is defined as minimum lithographic feature size", while claim 4 states that "the area occupied by said trench is greater than or equal to about F^2".

Claim 1 of U.S. Patent No. 6,025,624 includes as the first clause "a container capacitor having a storage electrode, the storage electrode having a width of 1F and a length greater than 4F, where F is the minimum

lithographic dimension". Not only is the rejection improper, the Examiner is noticeably inconsistent in applying these newly-minted principles of patent law.

The Office is unable to point to any change in the regulations under 37 C.F.R.; legislative changes under 35 U.S.C. or any amendments to the MPEP that would permit the Office to take such a drastic change in direction. Consequently, Applicant by and through their attorney state the Office has engaged in a policy shift which violates the provisions of the Federal Constitution regarding Applicants' rights to equal protection under the law.

For at least these reasons, the rejection of claims 44, 45, 51-54, 56, 58-60, 62 and 66-68 under 35 U.S.C. §112, first paragraph, is clearly erroneous and should be withdrawn, and claims 44, 45, 51-54, 56, 58-60, 62 and 66-68 should be allowed.

Issue 2.

Each of Applicants' independent claims provides affirmative and definite recitation of the claimed subject matter. For example, claim 44 recites "A pair of adjacent stacked capacitors fabricated using a photolithographic process having a characteristic minimum photolithographic feature dimension on a semiconductor substrate, the adjacent stacked capacitors respectively including a lower plate having a minimum lateral spacing from one another which is less than the minimum photolithographic feature dimension, each lower plate including a polysilicon plug having a diameter less than the minimum photolithographic feature dimension."

Extrinsic Evidence Of Clarity and Usage of Language in the art

The terminology "minimum feature size" appears in at least 238 patents that have issued from the USPTO from January 1998 to the present, and some 600+ patents overall. Examples where such terms are used in claims to provide meaningful and lawful definition of a properly-claimed invention include U.S. Patent Nos. 5,945,704; 5,945,688; 5,953,254; 5,968,686; and 5,907,170. This is extrinsic evidence that the terms used in Applicants' claims put the public on adequate notice as to the claimed subject matter, that these terms are understood and that these terms are used to define statutory subject matter.

Inconsistent Application of Arbitrary Standards

Additionally, as noted above, the name of the Examiner making this rejection also appears on U.S. Patent No. 6,150,687, issued to Noble et al., entitled "Memory Cell Having A Vertical Transistor With Buried Source/Drain And Dual Gates", filed on July 8, 1997; U.S. Patent No. 6,037,620, issued to Hoenigschmid et al., entitled "DRAM Cell With Transfer Device Extending Along Perimeter Of Trench Storage Capacitor", filed on June 8, 1998; and U.S. Patent No. 6,025,624, issued to Figura, entitled "Shared Length Cell For Improved Capacitance", filed on June 19, 1998.

Each of these patents resulted from an application that was filed after the instant application. Further, each of these patents state on their face that they were examined under the aegis of Examiner S. Crane. Each of these patents includes recitation of a "minimum feature size" or language equivalent thereto in defining the subject matter claimed, as noted with

particularity hereinabove. Not only is the rejection improper, the Examiner is noticeably inconsistent in applying these newly-minted principles of patent law.

The Examiner states that the phrase "minimum lithographic feature dimension" is indefinite. If that were so, why would this language be employed so widely in the lithographic arts and in patents, including patents that matured from applications filed after the instant application and which further were examined under the aegis of Examiner Crane as evidenced by her name appearing on their cover sheets? This language is clear, is well understood and is widely used by those familiar with the relevant arts.

The Examiner states that the term "photolithographic process" is not clear, because one cannot determine what wavelength the photons are that are being used in the process. What relevance does this have to the claimed subject matter? The term "photolithographic process" is abundantly clear, and again, is well and widely understood by those of skill in the arts.

Applicants believe that the pending claims are fully compliant with all requirements of 35 U.S.C. §112. The techniques developed by Applicants are described with sufficient clarity that any person of ordinary skill in the art is enabled to practice the present invention, irrespective of the lithographic technique that is employed. Further, the terms with which the invention is described and claimed are definite. For at least these reasons, the rejections under 35 U.S.C. §112, second paragraph, should be withdrawn, and claims 44, 45, 51-54, 56, 58-60 and 66-68 should be allowed.

Issue 3.

Claim 44 recites, in part, that "each lower plate including a polysilicon plug having a diameter less than the minimum photolithographic feature dimension" which is not taught, disclosed, suggested or motivated by the cited references, alone or in any proper combination.

Standard for making an Unpatentability Rejection

Simply stating a conclusion that "it would have been obvious" to combine teachings from references does not meet the standards for a rejection under 35 U.S.C. §103(a) as set forth in The Manual of Patent Examination Procedure at §706.02(j) entitled "Contents of a 35 U.S.C. 103 Rejection." This MPEP section states that three basic criteria must be met in order to establish a prima facie case of obviousness.

The first of these is that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. The Office Action fails to show that the subject matter of claim 44 is suggested or motivated by the teachings of the references.

The second requirement of MPEP §706.02(j) is that there must be a reasonable expectation of success. The third requirement is that the prior art reference (or references when combined) must teach or suggest all of the claim limitations.

Since all of the cited references are silent with respect to any polysilicon plug having a diameter less than the minimum photolithographic

feature dimension, combining their teachings cannot possibly provide the invention as recited in claim 44.

Further, because the references are silent with respect to polysilicon plugs having a diameter less than the minimum photolithographic feature dimension, there can be no reasonable expectation of success in arriving at the claimed subject matter from combining their teachings.

No Evidence Of Suggestion

Further, no evidence has been provided as to why it would be obvious to combine the teachings of any of these references. Evidence of a suggestion to combine may flow from the prior art references themselves, from the knowledge of one skilled in the art, or from the nature of the problem to be solved. However, this range of sources does not diminish the requirement for actual evidence. Further, the showing must be clear and particular. See *In re Dembiczak*, 175 F.3d 994, 998 (Fed. Cir. 1999).

'Obvious to Try' Is Not A Standard For Demonstrating Unpatentability

Applicants also note MPEP §2145, entitled "Consideration of Applicant's Rebuttal Arguments". This MPEP section states, in subsection B, entitled "Obvious To Try Rationale", that "An applicant may argue the examiner is applying an improper "obvious to try" rationale in support of an obviousness rejection.

The admonition that 'obvious to try' is not the standard under Section 103 has been directed mainly at two kinds of error. In some cases, what would have been 'obvious to try' would have been to vary all parameters or

try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful.

In others, what was 'obvious to try' was to explore a new technology or general approach that seemed to be a promising field of experimentation, where the prior art gave only general guidance as to the particular form of the claimed invention or how to achieve it." *In re O'Farrell*, 853 F.2d 894, 903, 7 USPQ2d 1673, 1681 (Fed. Cir. 1988) (citations omitted) (The court held the claimed method would have been obvious over the prior art relied upon because one reference contained a detailed enabling methodology, a suggestion to modify the prior art to produce the claimed invention, and evidence suggesting the modification would be successful.). See the cases cited in *O'Farrell* for examples of decisions where the court discussed an improper "obvious to try" approach. See also *In re Eli Lilly & Co.*, 902 F.2d 943, 14 USPQ2d 1741 (Fed. Cir. 1990) and *In re Ball Corp.*, 925 F.2d 1480, 18 USPQ2d 1491 (Fed. Cir. 1991) (unpublished) for examples of cases where appellants argued that an improper "obvious to try" standard was applied, but the court found that there was proper motivation to modify the references."

In the instant case, the Examiner offers (p. 5 of the Office Action dated August 29, 2000) the notion that "it would have been obvious in view of the art cited to make semiconductor structures smaller in order to fit more devices on a chip." This is wide of the mark of demonstrating obviousness, because the Examiner has failed to show any guidance whatsoever <u>in the references</u> that would lead one to the claimed structures.

For at least these reasons, the rejection of claim 44 should be withdrawn, and claim 44 should be allowed.

Issue 4.

Claim 45 recites "the adjacent stacked capacitors respectively including a lower plate having a minimum lateral spacing from one another which is less than the minimum photolithographic feature dimension wherein each of the pair of capacitors comprises: a polysilicon plug having a diameter less than the minimum photolithographic feature dimension; and in cross-section, at least two laterally opposed fins interconnected with and projecting laterally from the plug", which is not taught, disclosed, suggested or motivated by the cited references, alone or in any proper combination.

As noted above, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. The proposed combination fails to teach or suggest all of the claim limitations. For at least these reasons, the rejection of claim 45 should be withdrawn, and claim 45 should be allowed.

Claim 54 recites "the adjacent stacked capacitors respectively including a lower plate having a minimum lateral spacing from one another which is less than the minimum photolithographic feature dimension, each lower plate comprising a polysilicon plug having a diameter that is less than the minimum photolithographic feature dimension and, in cross-section, at least two laterally opposed fins interconnected with and projecting laterally from the plug", which is not taught, disclosed, suggested or motivated by the cited

references. For at least these reasons, the rejection of claim 54 should be withdrawn, and claim 54 should be allowed.

Claim 62 recites that "each finned lower plate comprises: a polysilicon plug; and in cross-section, at least two laterally opposed fins interconnected with and projecting laterally from the plug, the plug having a minimum width which is less than the minimum photolithographic feature dimension", which is not taught, disclosed, suggested or motivated by the cited references. For at least these reasons, the rejection of claim 62 should be withdrawn, and claim 62 should be allowed.

No Evidence Of Suggestion

Further, no evidence has been provided as to why it would be obvious to combine the teachings of any of these references. Evidence of a suggestion to combine may flow from the prior art references themselves, from the knowledge of one skilled in the art, or from the nature of the problem to be solved. However, this range of sources does not diminish the requirement for actual evidence. Further, the showing must be clear and particular. See *In re Dembiczak*, 175 F.3d 994, 998 (Fed. Cir. 1999).

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In others, what was 'obvious to try' was to explore a new technology or general approach that seemed to be a promising field of experimentation, where the prior art gave only general guidance as to the particular form of the claimed invention or how to achieve it." *In re O'Farrell*, 853 F.2d 894, 903, 7 USPQ2d 1673, 1681 (Fed. Cir. 1988) (citations omitted) (The court held the claimed method would have been obvious over the prior art relied upon because one reference contained a detailed enabling methodology, a suggestion to modify the prior art to produce the claimed invention, and evidence suggesting the modification would be successful.). See the cases cited in *O'Farrell* for examples of decisions where the court discussed an improper "obvious to try" approach. See also *In re Eli Lilly & Co.*, 902 F.2d 943, 14 USPQ2d 1741 (Fed. Cir. 1990) and *In re Ball Corp.*, 925 F.2d 1480, 18 USPQ2d 1491 (Fed. Cir. 1991) (unpublished) for examples of cases where appellants argued that an improper "obvious to try" standard was applied, but the court found that there was proper motivation to modify the references."

In the instant case, the Examiner offers (p. 5 of the Office Action dated August 29, 2000) the notion that "it would have been obvious in view of the art cited to make semiconductor structures smaller in order to fit more

devices on a chip." This is wide of the mark of demonstrating obviousness, because the Examiner has failed to show any guidance whatsoever in the references that would lead one to the claimed structures.

For at least these reasons, the rejection of claims should be withdrawn, and claims 45, 51-54, 56, 58-60 and 66-68 should be allowed.

CONCLUSION

The Examiner's rejection of claims 44, 45, 51-54, 56, 58-60, 62 and 66-68 is not supported by the cited references, the laws of the United States, any Federal regulatory documents or by the case law interpreting the above, and should be reversed.

In view of the foregoing, reversal of the final rejection of claims 44, 45, 51-54, 56, 58-60, 62 and 66-68 is respectfully requested.

Respectfully submitted,

Dated: July 30, 2001 By: _____

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APPENDIX

44. A pair of adjacent stacked capacitors fabricated using a photolithographic process having a characteristic minimum photolithographic feature dimension on a semiconductor substrate, the adjacent stacked capacitors respectively including a lower plate having a minimum lateral spacing from one another which is less than the minimum photolithographic feature dimension, each lower plate including a polysilicon plug having a diameter less than the minimum photolithographic feature dimension.

45. A pair of adjacent stacked capacitors fabricated using a photolithographic process having a characteristic minimum photolithographic feature dimension on a semiconductor substrate, the adjacent stacked capacitors respectively including a lower plate having a minimum lateral spacing from one another which is less than the minimum photolithographic feature dimension wherein each of the pair of capacitors comprises:

a polysilicon plug having a diameter less than the minimum photolithographic feature dimension; and

in cross-section, at least two laterally opposed fins interconnected with and projecting laterally from the plug.

51. The capacitors of claim 44, wherein the lower plates are formed from conductive polysilicon.

52. The capacitors of claim 45, wherein the plug and fins are formed from conductive polysilicon.

53. The capacitors of claim 45, wherein the pair of stacked capacitors are coated with a capacitor dielectric layer.

54. A pair of adjacent stacked capacitors fabricated using a photolithographic process having a characteristic minimum photolithographic feature dimension on a semiconductor substrate, the adjacent stacked capacitors respectively including a lower plate having a minimum lateral spacing from one another which is less than the minimum photolithographic feature dimension, each lower plate comprising a polysilicon plug having a diameter that is less than the minimum photolithographic feature dimension and, in cross-section, at least two laterally opposed fins interconnected with and projecting laterally from the plug.

56. The capacitors of claim 54 wherein the plug includes a minimum width which is less than the minimum photolithographic feature dimension.

58. The capacitors of claim 54, wherein the lower plates are formed from conductive polysilicon.

59. The capacitors of claim 54, wherein the plug and fins are formed from conductive polysilicon.

60. The capacitors of claim 54, wherein the pair of stacked capacitors are coated with a capacitor dielectric layer.

62. A pair of adjacent stacked capacitors fabricated using a photolithographic process having a characteristic minimum photolithographic feature dimension on a semiconductor substrate, the adjacent stacked capacitors respectively including a finned lower plate having a minimum lateral spacing from one another which is less than the minimum photolithographic feature dimension wherein each finned lower plate comprises:

a polysilicon plug; and

in cross-section, at least two laterally opposed fins interconnected with and projecting laterally from the plug, the plug having a minimum width which is less than the minimum photolithographic feature dimension.

66. The capacitors of claim 62, wherein the lower plates are formed from conductive polysilicon.

67. The capacitors of claim 62, wherein the plug and fins are formed from conductive polysilicon.

68. The capacitors of claim 62, wherein the pair of stacked capacitors are coated with a capacitor dielectric layer.